

WeiQi (Eddie) Peng

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EDUCATION

University of Notre Dame | Notre Dame, IN

May 2028

Electrical Engineering (Minor: CDT) | GPA: 3.63

Relevant Coursework: Analog Circuits, Digital Integrated Circuits, Embedded Systems, Computational Physics, IC Fab (Spring)

The Ohio State University | Columbus, OH

2024-2025

Chemical Engineering | GPA: 3.85

TECHNICAL INTERESTS

Digital IC Design | AI Hardware | SoC Implementation | Post-Silicon Validation | Semiconductor Test & Characterization

WORK EXPERIENCE

Suyue Xinyi Technology Co., Ltd. | Shenzhen, China

May 2026 - Aug 2026

IC Test and PCB Design Intern

- Developed and debugged SY1000 ATE test programs for 74LS138 and SN74HC00 digital ICs, implementing continuity, functional, DC parametric/PPMU, and propagation-delay tests from device specifications.
- Characterized VIH/VIL, IIH/IIL, VOH/VOL, ICC, and tPHL/tPLH; debugged functional-test failures by analyzing channel maps, voltage levels, timing sets, test patterns, and DUT connections.
- Designed PCB schematics and layouts in Cadence OrCAD, including custom symbols/footprints, netlists, placement, routing, copper pours, vias, and manufacturing outputs.

RESEARCH

Shenzhen Research Institute of UESTC | Shenzhen, China

May 2026 - Aug 2026

Research Assistant - High-Speed Jitter Component Analysis

- Implemented and evaluated a dual-input neural-network model using eye diagrams and jitter-distribution data to estimate deterministic, random, periodic, and duty-cycle-distortion jitter in high-speed digital signals.
- Generated and processed 10.3125-Gbps PRBS-9 data in ADS and Python; validated the method with Tektronix DPO72004C measurements, achieving experimental R-squared values of 0.90-0.99 across jitter components.

Wireless Institute / Laneman Group | Notre Dame, IN

Jan 2026 - May 2026

Undergraduate Researcher

- Characterized campus Wi-Fi AP load with Raspberry Pi/SigCap sensors and evaluated Meta Quest 3 performance over Wi-Fi/CBRS using latency, jitter, retry-rate, and throughput measurements.

RELEVANT PROJECTS

Digital Integrated Circuits Course Projects | Notre Dame

Fall 2026

- Designed standard cells in a 0.5- μm technology, passing DRC, LVS, and parasitic-extraction checks in Cadence Virtuoso and Layout GXL; synthesized and implemented an 8-bit MIPS processor using Cadence Genus and Innovus.
- Currently designing a processor in SystemVerilog for implementation in a TSMC 180-nm process using the Cadence FlowKit, including ATPG in Modus, timing signoff in Tempus, and power analysis in Voltus.

Heads-Up Poker AI Research | edpoker.online

Jul 2026 - Present

- Built a heads-up no-limit hold'em AI in Rust that pairs a CFR-trained strategy table (322M iterations) with a real-time range-vs-range DCFR game solver, solving each decision within a 7-40 s compute and ~3.4 GB memory budget.
- Raised AIVAT win rate against GTO Wizard's benchmark AI from -44.8 to -13.5 bb/100 over 130,000+ hands via pre-registered A/B and per-hand randomized tests; the final version currently ranks #7 of 100+ on the public leaderboard.

TECHNICAL SKILLS

Programming and HDL: SystemVerilog, C, C++, Rust, Python, MATLAB

IC Design and EDA: Cadence Virtuoso, Genus, Innovus, Modus, Tempus, Voltus, Layout GXL, OrCAD, SPICE, ADS

Hardware and Test: RTL Synthesis, DRC/LVS, Parasitic Extraction, ATPG, Timing/Power Analysis, ATE/PPMU, PCB Design, Oscilloscope, Jitter Analysis, Raspberry Pi Pico